REMARKS

Claims 1-4 and 6 were examined and reported in the Office Action. Claims 4 and 6 are rejected. Claim 4 is canceled. Claim 6 is amended. Claims 1-3 and 6 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. §112

It is asserted in the Office Action that claim 4 is rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has canceled claim 4. Therefore the 35 U.S.C. §112, second paragraph rejection for claim 4 is moot.

II. 35 U.S.C. §102(b)

It is asserted in the Office Action that claims 4 and 6 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 4,914,577 issued to Stewart et al ("Stewart"). Applicant has canceled claim 4. Applicant respectfully traverses the aforementioned rejection regarding claim 6 for the following reasons.

According to MPEP §2131,

> '[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)).

Applicant's amended claim 6 contains the limitations of

> [a] method for a refresh operation of a semiconductor memory device including a cell area having N+1 number of unit cell blocks, each including M number of word lines which respectively are coupled to a plurality of unit cells; a predetermined cell block table for storing candidate information representing at least more than one candidate word line among M * (N+1) number of the word lines; and a tag block having N+1 number of unit tag tables for sensing a logical cell block address corresponding to N number of unit cell blocks to output a physical unit cell address corresponding to N+1 number of unit cell blocks, each having M number of registers for sensing an update of data, comprising: nullifying the N+1 number of unit tag tables; selecting all the N+1 number of unit tag tables; and storing each different logical unit cell block information in the N number of unit tag tables among the N+1 number of unit tag tables, wherein the N number of unit cell blocks are corresponded to the logical cell block address and one unit cell block is more added for accessing data with high speed.

In other words, a semiconductor memory device includes a cell area having N+1 number of unit cell blocks, each including M number of word lines; a predetermined cell block table for storing candidate information representing at least more than one candidate word line among M * (N+1) number of the word lines; and a tag block having N+1 number of unit tag tables for sensing a logical cell block address corresponding to N number of unit cell blocks to output a physical unit cell address corresponding to N+1 number of unit cell blocks. Accordingly, it is possible to access data with high speed so that a data restoration time does not affect seriously a data access time.

Distinguishable, Stewart does not teach, disclose or suggest a predetermined cell block table for storing candidate information representing at least more than one candidate word line among M * (N+1) number of word lines according to Applicant's claimed invention.

Therefore, since Stewart does not teach, disclose or suggest all of Applicant's amended claim 6 limitations, Applicant respectfully asserts that a *prima facie* rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Stewart. Thus, Applicant's amended claim 6 is not anticipated by Stewart.

Accordingly, withdrawal of the 35 U.S.C. §102(b) rejections for claims 4 and 6 are respectfully requested.

III. Allowable Subject Matter

Applicant notes with appreciation the Examiner's assertion that claims 1-3 are allowed. Applicant respectfully asserts that claims 1-3 and 6, as they now stand, are allowable for the reasons given above.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1-3 and 6, patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees. If a telephone interview would expedite the prosecution of this Application, the Examiner is invited to contact the undersigned at (310) 207-3800.

Respectfully submitted,

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Dated: May 23, 2007

By: _____
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

_____
Jean Svoboda Date: May 23, 2007